What is Claimed is:

1. An apparatus for protecting data outputted from a code read only memory (ROM), comprising:

a first encryption means for encrypting data outputted from the code ROM;

a second encryption means for generating a read enable signal through an encryption process; and

an output means for dumping out the encrypted data outputted from the first encryption means in response to the read enable signal outputted from the second encryption means.

2. The apparatus of claim 1, wherein the first encryption means including:

a multiple input signature analysis register (MISR) for compressing data outputted from the code ROM in synchronization with a clock signal; and

an initializing means for providing an initialization value to the MISR unit in response to a test enable signal and a reset signal.

3. The apparatus of claim 2, wherein the initializing means includes a transistor, which provides the initialization value to the MISR unit when all the test enable signal and the reset signal are enabled.

4. The apparatus of claim 1, wherein the second

encryption means including:

a control state machine unit for generating a control signal for a ROM test operation in response to the test enable signal and the clock signal;

a MISR unit for inputting, inputting and compressing key data in synchronization with the clock signal;

an initializing means for providing an initialization value to the MISR unit in response to the test enable signal and the reset signal; and

a comparison unit for outputting the read enable signal by comparing a value outputted from the MISR unit with an expected value.

5. The apparatus of claim 4, wherein the expected value is a value generated in a condition of recognizing the initialization value and the key data.

6. The apparatus of claim 4, wherein the control state machine unit includes an initial state, a finish state and a plurality of internal states, wherein the control state machine unit transits to the initial state in response to a reset signal, wherein the control state machine unit sequentially transits to a plurality of internal states in response to the test enable signal and the clock signal, wherein the control state machine unit in the final internal state, finally transits to the finish state, wherein the control state machine unit outputs the enabled control signal

in the initial state and in the plurality of internal states, and wherein the control state machine unit outputs the control signal in the final state.

7. The apparatus of claim 4, wherein the control state machine unit equips the internal state as much as the number of the key data.

8. The apparatus of claim 4, wherein the comparison means outputs the read enable signal when the compressing value outputted from the MISR unit and the initialization value are the same.

9. The apparatus of claim 4, wherein the initializing means includes a transistor, which provides the initialization value to the MISR unit when all the test enable signal and the reset signal are enabled.

10. The apparatus of claim 4, wherein the output means includes a logic multiplication means for ANDing the encrypted data outputted from the first encryption means and the read enable signal.

11. An apparatus for protecting data outputted from a code ROM, comprising:

a control state machine unit for generating a control signal for a ROM test operation in response to the test enable

signal and the clock signal;

a MISR unit for inputting, compressing key data in synchronization with the clock signal in response to the test enable signal;

an initializing means for providing an initialization value to the MISR unit in response to the test enable signal and the reset signal;

a comparison unit for outputting the read enable signal by comparing value outputted from the MISR unit with an expected value; and

an output means for dumping the code ROM data in response to a read enable signal.

12. The apparatus of claim 11, wherein the initialization value is a value generated in a condition of recognizing the initialization value and the key data.

13. The apparatus of claim 11, wherein the control state machine unit includes an initial state, a finish state and lots of internal states, and the control state machine unit transits to the initial state, the lots of internal states, sequentially, and to the finish state, finally, in response to a reset signal, the test enable signal and the clock signal, and in the final internal state, respectively, and then, the initial state and the lots of internal states output the enabled control signal, and the final state outputs disabled the control signal.

14. The apparatus of claim 11, wherein the control state machine unit equips the internal state as much as the number of the key data.

15. The apparatus of claim 11, wherein the comparison means outputs enabled the read enable signal when the compressing value outputted from the MISR unit and the initialization value are the same.

16. The apparatus of claim 11, wherein the initializing means includes a transistor, which provides the initialization value to the MISR unit when all the test enable signal and the reset signal are enabled.

17. The apparatus of claim 11, wherein the output means includes a logic multiplication means for ANDing the encrypted data outputted from the first encryption means and the read enable signal.